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Platon N. Mandros
BURNS, DOANE,
SWECKER & MATHIS, L.L.P.
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER	
WANG, QUAN ZHEN	
ART UNIT	**PAPER NUMBER**
2613	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,234	TOTSUKA ET AL.	
	Examiner	Art Unit	
	Quan-Zhen Wang	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 14-22* is/are allowed.

6)☒ Claim(s) *8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/9/02,8/18/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Varian (U.S. Patent US 5,392,289).

Regarding claim 8, Varian discloses a multiplexing circuit (figs. 2 and 8) comprising: an input interface (fig. 2, combination of 125 and 133) for inputting an electric signal; a multiplexing circuit (fig. 2, parallel to serial converter 230) for time-multiplexing the inputted electric signal; a pseudo-random pattern generator (fig. 2, PN generator 800 and fig. 8, PN generator/detector) for generating a pseudo-random pattern signal, and for outputting the pseudo-random pattern signal to the multiplexing circuit (fig. 2, parallel to serial converter 230); and a pseudo-random pattern detector (fig. 8, PN generator/detector) for evaluating the pseudo-random pattern signal, which has been inputted through the input interface (fig. 2, combination of 125 and 133).

Regarding claim 9, Varian further discloses that the pseudo-random pattern generator/detector is configured as one circuit comprising the pseudo-random pattern generator and the pseudo-random pattern detector (fig. 8, PN generator/detector 800).

Regarding claim 10, Varian discloses a demultiplexing circuit (figs. 3, 5, and 8) comprising: a demultiplexing circuit (fig. 3, serial to parallel converter 306) for

demultiplexing an inputted electric signal; an output interface (fig. 3, combination of all of the outputs on the right hand side of fig. 3) for outputting the demultiplexed electric signal; a pseudo-random pattern generator (fig. 3, correlator network 400; fig. 5, element 800; and fig. 8, PN generator/detector800) for generating a pseudo-random pattern signal, and for outputting the pseudo-random pattern signal to the output interface; and a pseudo-random pattern detector (fig. 3, correlator network 400; fig. 5, element 800; and fig. 8, PN generator/detector800)for evaluating the pseudo-random pattern signal, which has been inputted through the demultiplexing circuit (fig. 3, serial to parallel converter 306).

Regarding claim 11, Varian further discloses that the pseudo-random pattern generator/detector is configured as one circuit comprising the pseudo-random pattern generator and the pseudo-random pattern detector (fig. 8, PN generator/detector 800).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Varian (U.S. Patent US 5,392,289) in view of Platt (U.S. Patent US 5,802,073).

Regarding claim 12, Varian discloses a multiplexing circuit (figs. 2 and 8) comprising: an input interface (fig. 2, combination of 125 and 133) for inputting an

electric signal; a multiplexing circuit (fig. 2, parallel to serial converter 230) for time-multiplexing the inputted electric signal; a first pseudo-random pattern generator (fig. 2, PN generator 800 and fig. 8, PN generator/detector) for generating a pseudo-random pattern signal, and for outputting the pseudo-random pattern signal to the multiplexing circuit (fig. 2, parallel to serial converter 230); and a first pseudo-random pattern detector (fig. 8, PN generator/detector) for evaluating the pseudo-random pattern signal, which has been inputted through the input interface (fig. 2, combination of 125 and 133). Varian differs from the claimed invention in that Varian does not specifically disclose that the circuit further comprising a demultiplexing portion including: a demultiplexing circuit for demultiplexing the inputted electric signal; an output interface for outputting the demultiplexed electric signal; a second pseudo-random pattern generator for generating a pseudo-random pattern signal, and for outputting the pseudo-random pattern signal to the output interface; and a second pseudo-random pattern detector for evaluating the pseudo-random pattern signal, which has been inputted through the demultiplexing circuit. However, Varian discloses a demultiplexing circuit comprising a demultiplexing circuit (fig. 3, serial to parallel converter 306) for demultiplexing an inputted electric signal; an output interface (fig. 3, combination of all of the outputs on the right hand side of fig. 3) for outputting the demultiplexed electric signal; a pseudo-random pattern generator (fig. 3, correlator network 400; fig. 5, element 800; and fig. 8, PN generator/detector800) for generating a pseudo-random pattern signal, and for outputting the pseudo-random pattern signal to the output interface; and a pseudo-random pattern detector (fig. 3, correlator network 400; fig. 5, element 800; and fig. 8,

PN generator/detector800)for evaluating the pseudo-random pattern signal, which has been inputted through the demultiplexing circuit (fig. 3, serial to parallel converter 306). Varian further discloses that the multiplexing and demultiplexing circuits are used for a transmitter and receiver, respectively (fig. 1). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to incorporate the demultiplexing circuit with the multiplexing circuit in order to build a compact transceiver. The modified system of Varian further differs from the claimed invention in that Varian does not specifically disclose a loopback path that transmits the pseudo-random pattern signal from the multiplexing circuit to the demultiplexing circuit. However, a loopback path is well known in the art. For example, Platt discloses a loopback path (fig. 1A, loopback). Therefore, it would have been obvious for one of ordinary skill in the art at the time when the invention was made to incorporate a loopback path, as it is disclosed by Platt, in the modified system of Varian in order to provide self-testing functionality to the system.

Allowable Subject Matter

5. Claims 1-7, and 14-22 are allowed.

6. The following is an examiner's statement of reasons for allowance:

Claims 1-7 are allowable since the prior art of record does not teach or suggest in combination an optical transceiver comprising a transmitting side path including: an input interface for inputting an electric signal; a multiplexing circuit for time-multiplexing the inputted electric signal; and an electricity-light converter for converting the time-multiplexed electric signal into a light signal; and a receiving side path including: a light-

electricity converter for converting an inputted light signal into an electric signal; a demultiplexing circuit for demultiplexing the converted electric signal; and an output interface for outputting the demultiplexed electric signal; wherein, in the transmitting side path, said optical transceiver comprises: a first pseudo-random pattern generator for generating a pseudo-random pattern signal, and for outputting the pseudo-random pattern signal to the multiplexing circuit; and a first pseudo-random pattern detector for evaluating the pseudo-random pattern signal, which has been inputted to the transmitting side path through the input interface; in the receiving side path, said optical transceiver comprises: a second pseudo-random pattern generator for generating a pseudo-random pattern signal, and for outputting the pseudo-random pattern signal to the output interface; and a second pseudo-random pattern detector for evaluating the pseudo-random pattern signal, which has been inputted to the receiving side path through the demultiplexing circuit; and said optical transceiver further comprising: a first loopback path that transmits the pseudo-random pattern signal from the multiplexing circuit of the transmitting side path to the demultiplexing circuit of the receiving side path; and a second loopback path that transmits the pseudo-random pattern signal from the light-electricity converter of the receiving side path to the electricity-light converter of the transmitting side path; in addition to other limitations cited in the claims.

Claims 14-16 are allowable since the prior art of record does not teach or suggest in combination a method for evaluating and testing an optical transceiver, said optical transceiver comprising: a transmitting side path including: an input interface for inputting an electric signal; a first pseudo-random pattern generator for generating a

pseudo-random pattern signal; a first pseudo-random pattern detector for evaluating the pseudo-random pattern signal, which has been inputted through the input interface; a multiplexing circuit for time-multiplexing the inputted electric signal; an electricity-light converter for converting the time-multiplexed electric signal into a light signal; a receiving side path including: a light-electricity converter for converting an inputted light signal into an electric signal; a demultiplexing circuit for demultiplexing the converted electric signal; and a second pseudo-random pattern generator for generating a pseudo-random pattern signal; a second pseudo-random pattern detector for evaluating the pseudo-random pattern signal, which has been inputted through the demultiplexing circuit; and an output interface for outputting the demultiplexed electric signal; a first loopback path that transmits the pseudo-random pattern signal from the multiplexing circuit of the transmitting side path to the demultiplexing circuit of the receiving side path; and a second loopback path that transmits the pseudo-random pattern signal from the light-electricity converter of the receiving side path to the electricity-light converter of the transmitting side path; wherein: the optical transceiver is placed on an implementation substrate; a loopback electric wiring is placed on the implementation substrate so that said loopback electric wiring loops back from an output electric wiring on the implementation substrate, which is connected to the output interface, to an input electric wiring on the implementation substrate, which is connected to the input interface; an output of the electricity-light converter is connected to an outside pseudo-random pattern detecting function through a first optical fiber; and an input of a light-

electricity converter is connected to an outside pseudo-random pattern generating function through a second optical fiber; in addition to other limitation cited in the claims.

Claims 17-19 are allowable since the prior art of record does not teach or suggest in combination a method for evaluating and testing an optical transceiver, said optical transceiver comprising: a transmitting side path including: an input interface for inputting an electric signal; a first pseudo-random pattern generator for generating a pseudo-random pattern signal; a first pseudo-random pattern detector for evaluating the pseudo-random pattern signal, which has been inputted through the input interface; a multiplexing circuit for time-multiplexing the inputted electric signal; and an electricity-light converter for converting the time-multiplexed electric signal into a light signal; a receiving side path comprising: a light-electricity converter for converting an inputted light signal into an electric signal; a demultiplexing circuit for demultiplexing the converted electric signal; a second pseudo-random pattern generator for generating a pseudo-random pattern signal; a second pseudo-random pattern detector for evaluating the pseudo-random pattern signal, which has been inputted through the demultiplexing circuit; and an output interface for outputting the demultiplexed electric signal; and a loopback path that transmits the pseudo-random pattern signal from the multiplexing circuit of the transmitting side path to the demultiplexing circuit of the receiving side path; wherein: the optical transceiver is placed on an implementation substrate; a loopback electric wiring is placed on the implementation substrate so as to loop back from an output electric wiring on the implementation substrate, which is connected to the output interface, to an input electric wiring on the implementation substrate, which is

connected to the input interface; a loopback optical fiber, which is used for transmitting the pseudo-random pattern signal from a first optical fiber connected to an output of the electricity-light converter to a second optical fiber connected to an input of the light-electricity converter, is connected; the input electric wiring on the implementation substrate is connected to an outside pseudo-random pattern generating function; and the output electric wiring on the implementation substrate is connected to an outside pseudo-random pattern detecting function; in addition to other limitation cited in the claims.

Claims 20-22 are allowable since the prior art of record does not teach or suggest in combination a method for evaluating and testing an optical transceiver, said optical transceiver comprising: a transmitting side path including: an input interface for inputting an electric signal; a first pseudo-random pattern generator for generating a pseudo-random pattern signal; a first pseudo-random pattern detector for evaluating the pseudo-random pattern signal, which has been inputted through the input interface; a multiplexing circuit for time-multiplexing the inputted electric signal; and an electricity-light converter for converting the time-multiplexed electric signal into a light signal; a receiving side path including: a light-electricity converter for converting an inputted light signal into an electric signal; a demultiplexing circuit for demultiplexing the converted electric signal; and a second pseudo-random pattern generator for generating a pseudo-random pattern signal; a second pseudo-random pattern detector for evaluating the pseudo-random pattern signal, which has been inputted through the demultiplexing circuit; and an output interface for outputting the demultiplexed electric signal; and a

loopback path that transmits the pseudo-random pattern signal from the multiplexing circuit of the transmitting side path to the demultiplexing circuit of the receiving side path; wherein: the optical transceiver is placed on an implementation substrate; a loopback electric wiring is placed on the implementation substrate so as to loop back from an output electric wiring on the implementation substrate, which is connected to the output interface, to an input electric wiring on the implementation substrate, which is connected to the input interface; and a loopback optical fiber, which is used for transmitting the pseudo-random pattern signal from a first optical fiber connected to an output of the electricity-light converter to a second optical fiber connected to an input of the light-electricity converter, is connected; in addition to other limitation cited in the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ramamurthy et al. (U.S. Patent US 5,787,114) disclose a loop-back test system and method. Mukherjee et al. (N. Mukherjee et al. "Built-in self-test: a complete test solution for telecommunication systems", IEEE Communications

Magazine, June 1999, pages 72-78) disclose a method for built-in self-test targeted toward telecommunication systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan-Zhen Wang whose telephone number is (571) 272-3114. The examiner can normally be reached on 9:00 AM - 5:00 PM, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

qzw
9/28/06

JASON CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600